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DOCKET NO.: 1263-0013US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:	§	
	§	
Deepak Mehta et al.	§	Confirmation No.: 7292
	§	
Application No.: 09/981,954	§	Art Unit: 2123
	§	
Filed: 10/18/2001	§	Examiner: Kandasamy Thangavelu

For: SYSTEM AND METHOD FOR MEMORY COMPILER CHARACTERIZATION

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Shreen K. Danamraj

Dear Sir:

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Pursuant to 37 C.F.R. §41.37, Applicant (hereinafter "Appellant") hereby submits an appeal brief in the above-captioned patent application within the requisite time, as extended by way of a Petition for Extension attached herewith, from the date of filing of the Notice of Appeal which was filed on June 9, 2006.

This appeal is from the decision of Examiner Kandasamy Thangavelu, Art Unit 2123, rejecting claims 1-7, 14-21, and 28-45.

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in the present patent application, as set forth in the Final Office Action dated January 20, 2006.

I. REAL PARTY IN INTEREST

The real party in interest of the present patent application is Virage Logic Corp., a corporation organized and existing under the laws of the State of California, having its principal place of business at 47100 Bayside Parkway, Fremont, CA 94538.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any other prior and/or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by or otherwise have a bearing on the Board's decision in this pending appeal.

III. STATUS OF CLAIMS

Claims 1-7, 14-21 and 28-45 are currently pending, of which claims 1, 16, and 35 are in independent form.

Claims 1, 5-7, 14-15, 35-38, and 45 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,405,160 to Djaja et al. (hereinafter the *Djaja* reference).

Claims 2-4 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of U.S. Patent No. 6,249,901 to Yuan et al. (hereinafter the *Yuan* reference).

Claims 16, 20-21, 28-34, and 39-44 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of U.S. Patent No. 5,175,707 to Murotani (hereinafter the *Murotani* reference).

Claims 17-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of the *Murotani* reference and further in view of the *Yuan* reference.

Claims 1-7, 14-21 and 28-45 are on appeal.

IV. STATUS OF AMENDMENTS

Set forth below is a synopsis of the chronology with respect to claim amendments:

A First Office Action on the merits was mailed on June 17, 2005 rejecting claims 1-49 variously based on 35 U.S.C. §101, 35 U.S.C. §102(e), and 35 U.S.C. §103(a). The *Djaja*, *Murotani*, and *Yuan* references were applied with respect to the art-based rejections of the Office Action.

Appellant filed a Response on December 19, 2005 in which claims 8-13, 22-27, and 46-48 were canceled; and pending base

claims 1, 16, and 35 were amended, among others. Appellant argued that the pending claims as amended were distinguishable over the art of record.

A Final Office Action was mailed on January 20, 2006 which maintained the rejection of claims 1-7, 14-21 and 28-45 variously based on 35 U.S.C. §102(e) and 35 U.S.C. §103(a). The *Djaja*, *Murotani*, and *Yuan* references continued to be applied with respect to the art-based rejections of the Office Action.

Appellant filed a Notice of Appeal on June 9, 2006 in response.

A copy of the claims relating to this appeal is attached hereto as an Appendix.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A concise explanation of the subject matter defined in each of the appealed independent claims is set forth in this Section, including appropriate references to the specification, e.g., by page and line number, reference numerals in drawings, etc. These specific references are examples of particular elements of the drawings for certain embodiments of the claimed invention, and the claims are not limited solely to the elements corresponding to the applied reference numerals.

Independent claim 1 is directed to an embodiment of a memory compiler characterization method for determining parametric data associated with compilable memory instances (see, e.g., FIGS. 3 and 5 and related description in the specification at paragraphs [0040]-[0041] and [0044]; see also FIG. 1 and related description in the specification at paragraphs [0020]-[0032]). The claimed embodiment comprises obtaining a first parametric dataset (e.g., dataset 102A in FIG. 1) associated with a first plurality of memory compilers, the memory compilers for compiling a first set of memory instances, each instance having a select number of physical rows and a select number of physical columns, wherein each memory instance is organized using a first MUX factor and further wherein a data point in the first parametric dataset corresponds to a value

with respect to a particular parameter characterized for a memory instance sampled from the first set of memory instances (see, e.g., paragraphs [0021]-[0028] of the specification; see also block 302 in FIG. 3 and block 502 in FIG. 5). Also included in the claimed embodiment is the operation of obtaining a sparsely populated second parametric dataset (e.g., dataset 102B in FIG. 1) by characterizing the particular parameter for a second set of memory instances that are compiled by a second plurality of memory compilers, each of the second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor, wherein the second plurality of memory compilers are sampled from the first plurality of memory compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory instance of the first parametric dataset (e.g., dataset 102A in FIG. 1) having identical numbers of physical rows and physical columns (see, e.g., paragraphs [0029]-[0030] of the specification; see also block 304 in FIG. 3 and block 504 in FIG. 5). Appropriate scale factors are determined for a select number of parametric data points associated with respective congruent memory instances of the first and second parametric datasets 102A and 102B (see, e.g., paragraph [0031] of the specification; see also block 306 in FIG. 3 and block 506 in

FIG. 5). An interpolated scale factor is obtained based on the scale factors (see, e.g., paragraph [0032] of the specification; see also block 308 in FIG. 3 and block 508 in FIG. 5). The claimed embodiment then includes filling in the second parametric dataset 102B by deriving a value of the particular parameter for an additional memory instance having the second MUX factor upon application of the interpolated scale factor to a data point associated with a memory instance having the first MUX factor, wherein the memory instance with the first MUX factor is congruent with respect to the additional memory instance with the second MUX factor (see, e.g., paragraph [0032] of the specification; see also block 310 in FIG. 3 and block 510 in FIG. 5).

Independent claim 16 is directed to another embodiment of a memory compiler characterization method for determining parametric data associated with compilable memory instances wherein different technologies are scaled (see, e.g., FIGS. 4 and 5 and related description in the specification at paragraphs [0042]-[0043] and [0044]; see also FIG. 2 and related description in the specification at paragraphs [0034]-[0039]). The claimed embodiment comprises obtaining a first parametric dataset (e.g., 202A) associated with a first plurality of memory compilers representative of a first memory technology, the memory compilers

for compiling a first set of memory instances, each instance having a select number of physical rows and a select number of physical columns and organized using a select MUX factor, wherein a data point in the first parametric dataset 202A corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from the first set of memory instances (see, e.g., paragraphs [0034]-[0036] of the specification; see also block 402 in FIG. 4 and block 502 in FIG. 5). Also included in the claimed embodiment is obtaining a sparsely populated second parametric dataset (e.g., dataset 202B in FIG. 2) by characterizing the particular parameter for a second set of memory instances compiled by a second plurality of memory compilers that are representative of a second memory technology, each of the second plurality of memory compilers for compiling a respective memory instance organized with the same select MUX factor, wherein the second plurality of memory compilers are sampled from the first plurality of memory compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory instance of the first parametric dataset 202A having identical numbers of physical rows and physical columns (see, e.g., paragraph [0037] of the specification; see also block 404 in FIG. 4 and block 504 in FIG. 5). Appropriate scale factors

are determined for a select number of parametric data points associated with respective congruent memory instances of the first and second parametric datasets 202A and 202B (see, e.g., paragraph [0038] of the specification; see also block 406 in FIG. 4 and block 506 in FIG. 5). An interpolated scale factor is obtained based on the scale factors (see, e.g., paragraph [0039] of the specification; see also block 408 in FIG. 4 and block 508 in FIG. 5). The claimed embodiment then includes filling in the second parametric dataset 202B by deriving a value of the particular parameter for an additional memory instance of the second memory technology upon application of the interpolated scale factor to a data point associated with a memory instance of the first memory technology, wherein the memory instance of the first memory technology is congruent with respect to the additional memory instance of the second memory technology (see, e.g., paragraph [0039] of the specification; see also block 410 in FIG. 4 and block 510 in FIG. 5).

Independent claim 35 is directed to an embodiment of a memory compiler characterization system (see, e.g., FIG. 5 and related description in the specification at paragraph [0044]). The claimed embodiment comprises means for characterizing a first plurality of memory compilers with respect to a particular parameter, the first

plurality of memory compilers for compiling memory instances of a first type (see, e.g., block 502 of FIG. 5; see also related description in the specification). Also included in the claimed embodiment are means for characterizing a second plurality of memory compilers with respect to the particular parameter, the second plurality of memory compilers for compiling memory instances of a second type, wherein the memory instances of second type comprise memory instances sparsely sampled from the memory instances of first type such that each sampled memory instance of second type corresponds to a respective congruent memory instance of first type having identical numbers of physical rows and physical columns (see, e.g., block 504 of FIG. 5; see also related description in the specification) and means for determining scale factors between values of the particular parameter respectively associated with a pair of congruent memory instances of the first and second types (see, e.g., block 506 of FIG. 5; see also related description in the specification). An interpolator is provided to obtain an interpolated scale factor based on the scale factors (see, e.g., block 508 of FIG. 5; see also related description in the specification). Also included is means for obtaining a value of the particular parameter for an additional memory instance of second type by utilizing the interpolated scale factor in

conjunction with a parametric value of a congruent memory instance of first type which corresponds to the additional memory instance (see, e.g., block 510 of FIG. 5; see also related description in the specification).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Claims 1, 5-7, 14-15, 35-38, and 45 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,405,160 to Djaja et al. (hereinafter the *Djaja* reference).

(2) Claims 2-4 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of U.S. Patent No. 6,249,901 to Yuan et al. (hereinafter the *Yuan* reference).

(3) Claims 16, 20-21, 28-34, and 39-44 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of U.S. Patent No. 5,175,707 to Murotani (hereinafter the *Murotani* reference).

(4) Claims 17-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of the *Murotani* reference and further in view of the *Yuan* reference.

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VII. ARGUMENT

A. Argument with respect to base claims 1 and 35, and dependent claims 5-7 and 14-15 depending from base claim 1 and dependent claims 36-38 and 45 depending from base claim 35

In maintaining the §102(e) rejections of base claims 1 and 35 in the pending Final Office Action, the Examiner has commented as follows with specific regard to the *Djaja* reference as applied to base claim 1:

> **Djaja et al.** teaches Memory compiler interface and methodology. Specifically, as per claim 1, **Djaja et al.** teaches a memory compiler characterization method for determining parametric data associated with compilable memory instance (Abstract, L1-8; Fig. 2, Item 70; CL1, L5-12; Fig. 4; CL1, L55-57; CL4, L64-67), comprising:
>
> obtaining a first parametric dataset associated with a first plurality of memory compilers, the memory compilers for compiling a first set of memory instances, each instance having a select number of physical rows and a select number of physical columns (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20), wherein each memory instance is organized using a first MUX factor and further wherein a data point in the first parametric dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from the first set of memory instance (Abstract, L1-8; CL5, L13-20);
>
> obtaining a second parametric dataset by characterizing the particular parameter for a second set of memory instances that are compiled by a second plurality of memory compilers (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), each of the second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor (Abstract, L1-4 and L6-8), wherein the second plurality of memory compilers are sampled from the first plurality of memory

> compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory instance of the first parametric dataset having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31);
>
> determining scale factors for a select number of parametric data points associated with respective congruent memory instances of the first and second parametric datasets (Fig. 4, corner vertical lines; CL2, L46-47; CL4, L64-67; CL5, L52-65);
>
> obtaining an interpolated scale factor based on the scale factors (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle); and
>
> deriving a value of the particular parameter for an additional memory instance having the second MUX factor by applying the interpolated scale factor to a data point associated with a memory instance having the first MUX factor, wherein the memory instance with the first MUX factor is congruent with respect to the additional memory instance with the second MUX factor (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

In addition, substantially similar comments were made in the pending Office Action with respect to base claim 35, also rejected under 35 U.S.C. §102(e).

Appellant respectfully traverses the pending §102(e) rejections as set forth above and offers the following arguments in support. Base claim 1 is directed to a memory compiler characterization method which involves, *inter alia*, obtaining a first parametric dataset associated with a first plurality of

memory compilers that are used for compiling a first set of memory instances using a first MUX factor. Each data point in the first parametric dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from all possible memory configurations (e.g., varying number of rows and varying number of columns) comprising the first set of memory instances. A second parametric dataset is obtained by characterizing the same parameter for a second set of memory instances that are compiled by a second plurality of memory compilers, but with a second MUX factor. As claimed, the second plurality of memory compilers are sampled from the first plurality of memory compilers, in that not all memory configurations that were characterized in the first parametric dataset are characterized for the second parametric dataset. The scale factors are then determined for a select number of parametric data points associated with respective congruent memory instances (i.e., the memory instances having the same row X column configuration but with separate MUX factors). Based on the scale factors, an estimated scale factor is obtained, which is then used for deriving a parametric value of a memory instance with the second MUX factor that has not been characterized previously in the second parametric dataset. In other words, the parametric value of an additional

memory instance in the second dataset is not based on a 4-point interpolation of the corner data points surrounding the memory instance in the second dataset.

Similarly, base claim 35, directed to a memory compiler characterization system, involves, *inter alia*, means for charactering a second plurality of memory compilers with respect to a particular parameter, the second plurality of memory compilers for compiling memory instances of second type, wherein the memory instances of second type comprise memory instances sparsely sampled from the memory instances of first type such that only a subset of the memory instances of the first type correspond to the second type memory instances. Also included in the claimed embodiment are: means for determining scale factors between values of the particular parameters respectively associated with a pair of congruent memory instances of the first and second types; an interpolator to obtain an interpolated scale factor based on the scale factors; and means for obtaining a value of the particular parameter for an additional memory instance of the second type by utilizing the interpolated scale factor.

The *Djaja* reference is directed to a memory compiler for use in designing integrated memory arrays from user specifications. Essentially, the *Djaja* reference is concerned with statistical

modeling of memory parametric variables wherein each parametric variable is determined as a function of a number of memory architecture variables in obtaining what are referred to as characteristic equations by way of multivariate regression analysis. These characteristic equations are then used to predict the parametric values of a particular memory configuration supplied by the user.

As disclosed, the *Djaja* reference requires simulation of all possible memory configurations (i.e., matrix combinations of bits per word, number of rows, and column MUX factor) within a suitable range for purposes of determining the characteristic equations. See column 5, lines 47-65. As described in *Djaja*, a Full Factorial set with respect to a three variable analysis is shown in FIG. 4, inserted herein for convenience, wherein the three variables are: bits per word, number of rows, and column multiplexing factor. From FIG. 4, it can be readily seen that the dataset for the MUX 16 level comprises four corner points,

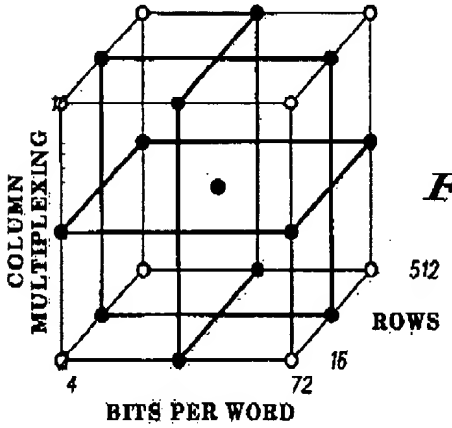

FIG. 4

represented by four white circles. Likewise, the dataset for the MUX 2 level also comprises four corner points on the bottom. As taught in *Djaja*, both MUX 16 level and MUX 2 level data points are obtained by known memory characterization techniques. See column 4, line 59 to column 5, line 12. Accordingly, there is no data point in the second parametric dataset, i.e., the MUX 2 level dataset, that has been interpolated from the neighboring data points in the MUX 2 level dataset. Nor is there a data point in the MUX 2 level dataset that has been derived based on applying an interpolated scale factor as claimed by Appellant. In other words, to the extent the datasets corresponding to two different levels (e.g., the bottom plane at MUX 2 and the top plane at MUX 16) of FIG. 4 of the *Djaja* reference can equated to the first and second parametric datasets as claimed by Appellant, as appears to be the case in the instant Final Office Action, the second parametric dataset is not obtained as a sparsely sampled set of data points with respect to the first parametric dataset since the datasets at MUX 2 and MUX 16 in *Djaja* are co-extensive. That is, for each data point characterized at MUX 2 level, there is also a corresponding data point characterized at MUX 16 level and vice versa, as shown in FIG. 4.

The Examiner appears to rely on the corner vertical lines of FIG. 4 (connecting the top white circles with the bottom white circles) in taking the position that these lines are anticipatory of "determining scale factors for a select number of parametric data points" as claimed Appellant. Further, the Examiner also takes the position that the darkened lines defining the horizontal plane in the middle of the cubicle in FIG. 4 (spanned by four dark circles) somehow teach "obtaining an interpolated scale factor based on said scale factors" as claimed by Appellant. See Final Office Action, pages 3 and 4. Appellant respectfully disagrees and asserts that, at a minimum, *Djaja* does not teach or allude to how "the corner vertical lines" give rise to a set of scale factors as claimed by Appellant. Nor does *Djaja* teach or suggest how "the lines defining the horizontal plane in the middle of the cubicle" can result in an interpolated scale factor that is applied to derive a data point in the MUX 2 level dataset.

The Examiner also contends in the instant Office Action at page 19 under the section ***Response to Arguments***:

> . . . the Examiner takes the position that the Djaja reference uses four point interpolation as used by the applicant. Therefore it performs simulations at the congruent points in the first parametric dataset and the second parametric dataset as performed by the applicant. While the applicant claims that "the second parametric dataset is obtained as a sparsely sampled set of data points with respect to the first parametric dataset", in

> reality he does the simulations at all points that are required for the four point interpolation as done by the Djaja reference. The Examiner does not see any difference between the method of Djaja reference and the applicant's method.

Appellant respectfully submits that there is not a single reference in *Djaja* with respect to "interpolation" of any kind, either in connection with the MUX 2 level dataset or with the MUX 16 level dataset, let alone obtaining an interpolated scale factor based on a set of scale factors between the two datasets and applying an estimated scale factor in order to derive a data point in the second parametric dataset. Contrary to the position taken by the Examiner, the claimed second parametric dataset is indeed sparsely populated with respect to the first parametric dataset: the total number of data points in the second dataset is considerably less than the total number of data points in the first dataset. See, e.g., paragraphs [0030] and [0033] of the specification.

At least for the foregoing reasons, Appellant respectfully submits that pending base claims 1 and 35 are allowable over the *Djaja* reference. Dependent claims 5-7 and 14-15 depend from base claim 1 and introduce further limitations therein. Likewise, dependent claims 36-38 and 45 depend from base claim 35 and introduce further limitations therein. Accordingly, it is believed

that these dependent claims are also allowable over the *Djaja* reference.

B. Argument with respect to dependent claims 2-4 depending from base claim 1

In the pending Office Action, dependent claims 2-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of the *Yuan* reference. Appellant incorporates by reference herein the argument set forth above in Part A with respect to the primary reference, i.e., the *Djaja* reference, and respectfully traverses the §103 rejection of claims 2-4 based thereon. As argued in the foregoing discussion, *Djaja* deficient at least with respect to certain limitations of base claim 1. Reliance on *Yuan*, however, does not cure the deficiencies of the *Djaja* reference. Accordingly, application of the *Yuan* reference is of no avail for purposes of maintaining a §103 rejection of a dependent claim under MPEP §2143 because not all of the claim limitations are taught or suggested in the combined teachings. It is therefore believed that dependent claims 2-4 are allowable over the art of record.

C. Argument with respect to base claim 16 and dependent claims 20-21 and 28-34 depending therefrom

In the pending Office Action, base claim 16 and dependent claims 20-21 and 28-34 depending therefrom are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of *Murotani*. In connection with these §103(a) rejections, the Examiner has commented as follows with respect to the primary reference:

> As per claim 16, **Djaja et al**. teaches a memory compiler characterization method for determining parametric data associated with compilable memory instances (Abstract, L1-8; Fig. 2, Item 70; CL1, L5-12; Fig. 4; CL1, L55-57; CL4, L64-67), comprising:
>
> obtaining a first parametric dataset associated with a first plurality of memory compilers, each of the memory compilers for compiling a respective memory instance having a select number of physical rows and a select number of physical columns (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20), and organized using a select MUX factor wherein a data point in the first parametric dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from the first set of memory instances (Abstract, L1-8; CL5, L13-20);
>
> obtaining a second parametric dataset by characterizing the particular parameter for a second set of memory instances compiled by a second plurality of memory compilers (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), each of the second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor (Abstract, L1-4 and L6-8), wherein a second plurality of memory compilers are sampled from the first plurality of memory compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory

> instance of the first parametric dataset having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31);
>
> determining scale factors for a select number of parametric data points associated with respective congruent memory instances of the first and second parametric datasets (Fig. 4, corner vertical lines; CL2, L46-47; CL4, L64-67; CL5, L52-65);
>
> obtaining an interpolated scale factor based on the scale factors (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle); and
>
> deriving a value of the particular parameter for an additional memory instance of second parametric dataset by applying the interpolated scale factor to a data point associated with a memory instance of the first parametric dataset, wherein the memory instance is congruent with respect to the additional memory instance of the second parametric dataset (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).
>
> **Djaja et al.** does not expressly teach that the first plurality of memory compilers are representative of a first memory technology; the second plurality of memory compilers are representative of a second memory technology. . .

Appellant incorporates by reference herein the argument set forth above in Part A with respect to the primary reference, i.e., the *Djaja* reference, and respectfully traverses the §103 rejection of claims 16, 20-21, and 28-34 claims based thereon. As argued in the foregoing discussion, *Djaja* deficient at least with respect to: obtaining a second parametric dataset that is sparsely populated in comparison to a first parametric dataset; determining scale factors

as between the first and second parametric datasets for a particular parameter; obtaining an interpolated scale factor based on the determined scale factors; and deriving a value of the particular parameter for an additional data point in the second parametric dataset by applying the interpolated scale factor. Application of the *Muratoni* reference, which is relied upon for its alleged teachings regarding different memory technologies, however, is of no avail for purposes of maintaining the §103 rejection of base claim 16 because it does not cure the deficiencies of the *Djaja* reference. In other words, the combined teachings of the *Djaja* and *Murotani* references do not anticipate or suggest all the limitations of base claim 16. Accordingly, Appellant respectfully submits that base claim 16 is in condition for allowance over the combination of *Djaja* and *Murotani* references. Further, it is believed that dependent claims 20-21 and 28-34 depending from base claim 16 are allowable over the art of record for the same reasons.

D. Argument with respect to dependent claims 39-44 depending from base claim 35

In the pending Office Action, dependent claims 39-44 depending from base claim 35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the *Djaja* reference in view of *Murotani*. Appellant incorporates by reference herein the argument set forth

above in Part A with respect to the primary reference, i.e., the *Djaja* reference, and respectfully traverses the §103 rejection of claims 39-44 based thereon. As argued in the foregoing discussion, *Djaja* deficient at least with respect to certain limitations of base claim 35. Application of the *Murotani* reference, however, is of no avail for purposes of maintaining a §103 rejection of a dependent claim under MPEP §2143 because not all of the claim limitations are taught or suggested in the combined teachings. Accordingly, it is believed that dependent claims 39-44 are allowable over the art of record.

E. Argument with respect to dependent claims 17-19 depending from base claim 16

In the pending Office Action, dependent claims 17-19 depending from base claim 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of the *Djaja*, *Murotani* and *Yuan* references. Appellant incorporates by reference herein the argument set forth above in Parts A and C with respect to the primary reference, i.e., the *Djaja* reference, and respectfully traverses the §103 rejection of claims 17-19 based thereon. As argued in the foregoing discussion, *Djaja* deficient at least with respect to certain limitations of base claim 16. Application of the *Murotani* and *Yuan* references, either together or in any

combination, however, is of no avail because the deficiencies of the primary reference are not cured. Accordingly, because not all of the claim limitations are taught or suggested in the combined teachings as required under MPEP §2143, it is believed that dependent claims 17-19 are allowable over the art of record.

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CHARGE STATEMENT:

All applicable fees are being paid along with this Appeal Brief. To the extent required, however, the Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fees(s) paid, or asserted to be filed, or which should have been filed herewith or concerning any paper filed as part of this transmittal to our **Deposit Account No. 03-1130.**

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CONCLUSION

In view of the foregoing discussion, Appellant respectfully submits that the rejection of the pending claims 1-7, 14-21 and 28-45 is not proper. Accordingly, Appellant respectfully requests that the rejection of the pending claims 1-7, 14-21 and 28-45 be overturned by the Board, and that the present patent application be allowed to issue as a patent with all pending claims.

Respectfully submitted,

Dated: 9/11/06

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VIII. APPEALED CLAIMS - APPENDIX

1. A memory compiler characterization method for determining parametric data associated with compilable memory instances, comprising:

obtaining a first parametric dataset associated with a first plurality of memory compilers, said memory compilers for compiling a first set of memory instances, each instance having a select number of physical rows and a select number of physical columns, wherein each memory instance is organized using a first MUX factor and further wherein a data point in said first parametric dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from said first set of memory instances;

obtaining a second parametric dataset by characterizing said particular parameter for a second set of memory instances that are compiled by a second plurality of memory compilers, each of said second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor, wherein said second plurality of memory compilers are sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds

to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns;

determining scale factors for a select number of parametric data points associated with respective congruent memory instances of said first and second parametric datasets;

obtaining an interpolated scale factor based on said scale factors; and

deriving a value of said particular parameter for an additional memory instance having said second MUX factor by applying said interpolated scale factor to a data point associated with a memory instance having said first MUX factor, wherein said memory instance with said first MUX factor is congruent with respect to said additional memory instance with said second MUX factor.

2. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said particular parameter comprises a memory timing parameter.

3. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 2, wherein said memory timing parameter comprises memory access time.

4. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 2, wherein said memory timing parameter comprises memory cycle time.

5. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said first MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

6. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said second MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

7. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein each memory instance of said first and second sets of memory instances comprises one of a read-only memory (ROM) circuit, a static random access memory (SRAM) circuit, a dynamic random access memory (DRAM) circuit, an electrically programmable ROM (EPROM) circuit, a flash memory circuit, an embedded memory circuit, and a stand-alone memory circuit.

14. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said interpolated scale factor is obtained by interpolating four scale factors, each corresponding to a ratio of values of said particular parameter for a pair of congruent memory instances.

15. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said first and second parametric datasets are obtained by characterization of said particular parameter via simulation.

16. A memory compiler characterization method for determining parametric data associated with compilable memory instances, comprising:

obtaining a first parametric dataset associated with a first plurality of memory compilers representative of a first memory technology, said memory compilers for compiling a first set of memory instances, each instance having a select number of physical rows and a select number of physical columns and organized using a select MUX factor, wherein a data point in said first parametric dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from said first set of memory instances;

obtaining a second parametric dataset by characterizing said particular parameter for a second set of memory instances compiled by a second plurality of memory compilers that are representative of a second memory technology, each of said second plurality of memory compilers for compiling a respective memory instance organized with said select MUX factor, wherein said second plurality of memory compilers are sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective

congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns;

determining scale factors for a select number of parametric data points associated with respective congruent memory instances of said first and second parametric datasets;

obtaining an interpolated scale factor based on said scale factors; and

deriving a value of said particular parameter for an additional memory instance of said second memory technology by applying said interpolated scale factor to a data point associated with a memory instance of said first memory technology, wherein said memory instance of said first memory technology is congruent with respect to said additional memory instance of said second memory technology.

17. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said particular parameter comprises a memory timing parameter.

18. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 17, wherein said memory timing parameter comprises memory access time.

19. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 17, wherein said memory timing parameter comprises memory cycle time.

20. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said select MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

21. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein each memory instance of said first and second sets of memory instances comprises one of a read-only memory (ROM) circuit, a static random access memory (SRAM) circuit, a dynamic random access memory (DRAM) circuit, an electrically programmable ROM (EPROM) circuit, a flash memory circuit, an embedded memory circuit, and a stand-alone memory circuit.

28. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said interpolated scale factor is obtained by interpolating four scale factors, each corresponding to a ratio of values of said particular parameter for a pair of congruent memory instances.

29. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first and second parametric datasets are obtained by characterization of said particular parameter via simulation.

30. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first memory technology is selected from at least one of 1.0μ technology, 0.8μ technology, 0.6μ technology and 0.2μ technology.

31. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said second memory technology is selected from at least one of 1.0μ technology, 0.8μ technology, 0.6μ technology and 0.2μ technology.

32. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first and second memory technologies comprise design-rule-specific technologies.

33. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first and second memory technologies comprise foundry-specific technologies.

34. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first and second memory technologies comprise process-flow-specific technologies.

35. A memory compiler characterization system, comprising:

means for characterizing a first plurality of memory compilers with respect to a particular parameter, said first plurality of memory compilers for compiling memory instances of a first type;

means for characterizing a second plurality of memory compilers with respect to said particular parameter, said second plurality of memory compilers for compiling memory instances of a second type, wherein said memory instances of second type comprise memory instances sparsely sampled from said memory instances of first type such that each sampled memory instance of second type corresponds to a respective congruent memory instance of first type having identical numbers of physical rows and physical columns;

means for determining scale factors between values of said particular parameter respectively associated with a pair of congruent memory instances of said first and second types;

an interpolator to obtain an interpolated scale factor based on said scale factors; and

means for obtaining a value of said particular parameter for an additional memory instance of second type by utilizing said interpolated scale factor in conjunction with a parametric value of a congruent memory instance of first type which corresponds to said additional memory instance.

36. The memory compiler characterization system as set forth in claim 35, wherein said memory instances of first type comprise memory instances with a first MUX factor and said memory instances of second type comprise memory instances with a second MUX factor.

37. The memory compiler characterization system as set forth in claim 36, wherein said first MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

38. The memory compiler characterization system as set forth in claim 36, wherein said second MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

39. The memory compiler characterization system as set forth in claim 35, wherein said memory instances of first type comprise memory instances associated with a first memory technology and said memory instances of second type comprise memory instances associated with a second memory technology.

40. The memory compiler characterization system as set forth in claim 39, wherein said first memory technology is selected from at least one of 1.0μ technology, 0.8μ technology, 0.6μ technology and 0.2μ technology.

41. The memory compiler characterization system as set forth in claim 39, wherein said second memory technology is selected from at least one of 1.0μ technology, 0.8μ technology, 0.6μ technology and 0.2μ technology.

42. The memory compiler characterization system as set forth in claim 39, wherein said first and second memory technologies comprise design-rule-specific technologies.

43. The memory compiler characterization system as set forth in claim 39, wherein said first and second memory technologies comprise process-flow-specific technologies.

44. The memory compiler characterization system as set forth in claim 39, wherein said first and second memory technologies comprise foundry-specific technologies.

45. The memory compiler characterization system as set forth in claim 35, wherein said memory instances comprise one of a DRAM circuit, an SRAM circuit, a ROM circuit, an EPROM circuit and a flash memory circuit.

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IX. EVIDENCE - APPENDIX

None.

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X. RELATED PROCEEDINGS - APPENDIX

None.